THREE INPUT VARIABLE SUBFIELD COMPARATION FOR FAST MATCHING

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ABSTRACT OF THE DISCLOSURE

The relationship between a sum of applied address operands and a matching virtual page number is exploited to minimize the adder size required for fast number comparison. In one embodiment, variably-sized addresses are accommodated by augmenting a portion of the applied address operands to ensure easy access to potential carry bits. A comparator is used for each virtual page number stored in a translation look-aside buffer to quickly determine whether that virtual page number matches the applied address operand sum.